GaAsFET Mount Structure Design for 30-GHz-Band Low-Noise Amplifiers

HIDEKI MIZUNO

Abstract—**This paper describes a GaAsFET mount design method for 30-GHz-band low-noise reflection-type amplifiers with the metal wall as a feedback circuit. Two examples of 30-GHz-band low-noise amplifiers are described; one with wide-band response and the other with high-gain response. The wide-band amplifier has 13-dB gain and 8.5-dB noise figure in the frequency range from 27.5 GHz to 29.1 GHz. The high gain amplifier has 15-dB gain and 9-dB noise figure in the frequency range from 27.7 GHz to 28.7 GHz. These results demonstrate the utility of this design approach.**

I. Introduction

IN RECENT YEARS, considerable attention has been given to the development of *Ka*-band low-noise GaAsFET amplifiers [1]–[4]. In *Ka*-band, circuit loss becomes a serious problem. Furthermore, the available gain per stage in these high-frequency regions becomes too small to ignore the influences of the second-stage noise figure.

The problem of circuit loss can be reduced with the use of a waveguide circuit instead of the MIC circuit. The problem of small gain per stage can be overcome by the employment of the negative resistance reflection-type amplifier configuration [1], [5]. In the FET amplifier, a feedback circuit is required to achieve the negative resistance characteristics. This circuit has to be located near a GaAsFET so as to achieve wideband performance.

This paper describes a GaAsFET mount design method for *Ka*-band low-noise amplifiers based on an analysis and experiment. The GaAsFET amplifier configuration is first presented. The design procedure is then described with examples.

II. GaAsFET Amplifier Structure

Fig. 1 shows the FET mount structure. The waveguide circuit is WRI-260 (8.636×4.318 mm). The FET mount is composed of waveguide input/output port, waveguide-to-coaxial line transition, gate load circuit, and a GaAsFET. The coaxial line characteristic impedance is 50 Ω at the gate and the drain. The dc bias is supplied through a coaxial line center conductor.

Fig. 2 shows the dimensions and their coordination for the FET housing section. The GaAsFET used in this amplifier is a 0.5-μm gate length device (2SK140) [See Table I]. This device is sealed in a stripline ceramic package. The drain lead is connected to the waveguide-to-coaxial line transition, while the gate lead is connected to a 50-Ω coaxial line, which is shorted at the other end. The source

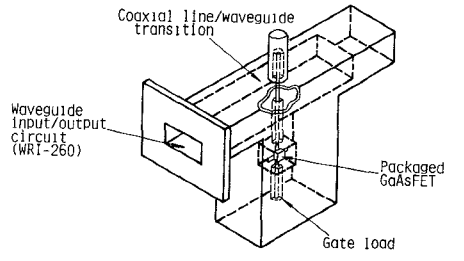

Fig. 1. FET mount structure.

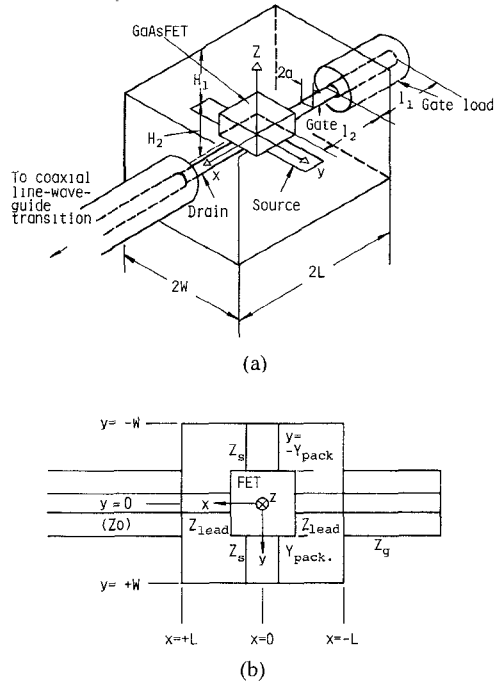

Fig. 2 FET mount structural details. (a) FET mount dimensions. (b) FET mount coordination.

TABLE I
GaAsFET Electrical Performance

Absolute Maximum Ratings		Electrical Characteristics			
V_{ds}	5.0 V	I_{dss}	50 mA	f_{max}	80 GHz
V_{gs}	-8.0 V	V_p	-2.5 V	NF	2.7 dB (@12GHz)
I_{ds}	100 mA	g_m	35 mS	MAG	11.0 dB (@12GHz)

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The author is with Yokosuka Electrical Communication Laboratory, Nippon Telegraph and Telephone, 1-2356, Take, Yokosuka-shi, Kanagawa-ken, 238-03, Japan.

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leads are connected to the metal wall of the FET mount.

The desired negative resistance characteristics can be achieved by adjusting the FET mount dimensions.

III. FET Mount Design Method

In this section, the mechanism of generating negative resistance with the FET mount is explained. The negative resistance frequency response and noise performance are then analyzed.

A. FET Mount Equivalent Circuit Model

The mounting scheme for the FET in a metal box is shown in Fig. 2. Looking into the right-hand side from the edge of the drain side coaxial line ($x = L$), it is evident that the FET mount is composed of the FET gate and drain lead portion (Z_{lead}), the FET package, the FET source lead grounding portion (Z_s), and the gate load (Z_g). An FET mount equivalent circuit model can be presented as shown in Fig. 3. Z_p is the stray reactance between the gate lead and the drain lead whose magnitude depends on the package dimensions. Z_s and Z_p form a feed back circuit in the FET amplifier.

Gate load Z_g is equal to the impedance of the line shorted at the other end. If the line is lossless, Z_g is given by

$$Z_g = jZ_{g0} \cdot \tan \beta l_1 \tag{1}$$

where Z_{g0} is the gate load line characteristic impedance; β is the propagation constant; and l_1 is the distance between short end and connected point.

The impedance at the gate end of the FET (Z_{gs}) is equal to that of the line impedance, whose characteristic impedance is Z_{lead}, length l_2 and termination Z_g. Then

$$Z_{gs} = \frac{Z_g + jZ_{\text{lead}} \cdot \tan \beta l_2}{jZ_g \cdot \tan \beta l_2 + Z_{\text{lead}}} Z_{\text{lead}}. \tag{2}$$

From (1) and (2)

$$Z_{gs} = j \frac{\sin(\beta l_1 + \phi_2)}{\cos(\beta l_1 + \phi_1)} Z_{\text{lead}} \tag{3}$$

where

$$\phi_1 = \tan^{-1}\left[(Z_{g0}/Z_{\text{lead}}) \tan \beta l_2\right]$$

$$\phi_2 = \tan^{-1}\left[(Z_{\text{lead}}/Z_{g0}) \tan \beta l_2\right].$$

Z_{gs} can be varied by changing Z_{lead} or l_1. l_1 can vary Z_{gs} more than Z_{lead} can.

FET gate and drain lead characteristics impedance Z_{lead} is equal to the characteristics impedance of the triplate stripline whose center conductor width is equal to package lead width $2a$, outer conductor width to FET mount width $2W$ and distances between center and outer conductors to the heights of the mount H_1 and H_2, respectively. Z_{lead} is calculated from Itoh's equations [6].

FET source lead grounding impedance Z_s is obtained experimentally. A parallel LC resonant circuit is assumed as Z_s. Z_s can be known by measuring the insertion loss between the mount input and output point when gate and drain are shorted. Fig. 4 (a) shows the insertion loss in the frequency range from 27 to 32 GHz. The solid line shows the calculated insertion loss when Z_s is approximated as a parallel LC resonant circuit. They show good agreement provided the approprite values of L and C are given. Fig. 4 (b) shows L and C as a function of Z_{lead}. Z_s can, therefore, be varied by varying Z_{lead}, that is, by changing W, H_1, and H_2.

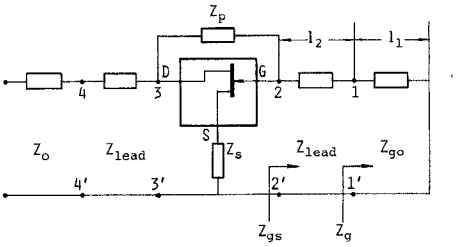
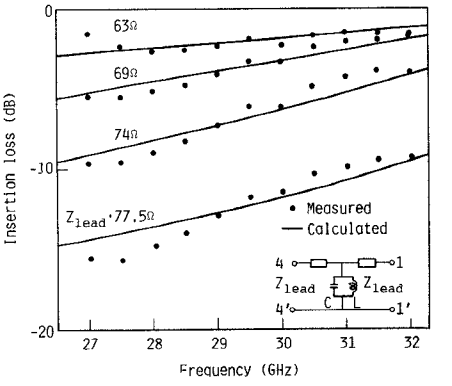
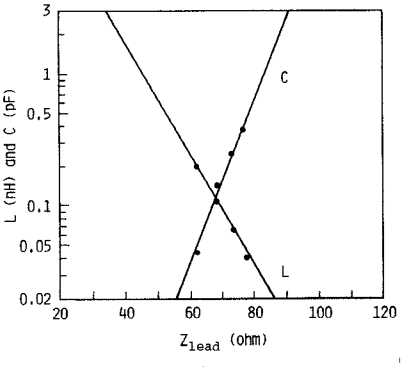


Fig. 3. FET mount equivalent circuit model.



(a)



(b)

Fig. 4. Insertion loss with varying Z_{lead}. (a) Measured and calculated results. (b) Variations of L and C values as a function of Z_{lead}.

B. Negative Resistance Characteristics Frequency Response

Utilizing the equivalent circuit element values obtained in Section III-A, the impedance of 4-4′ ports shown in Fig. 3 is calculated. Fig. 6 shows an example of the region where the negative resistance appears for the various mount

Z_p is included in the FET S-parameters shown in Fig. 5. The S-parameter values above 15 GHz are extrapolated from low-frequency region using the equivalent circuit of FET device.

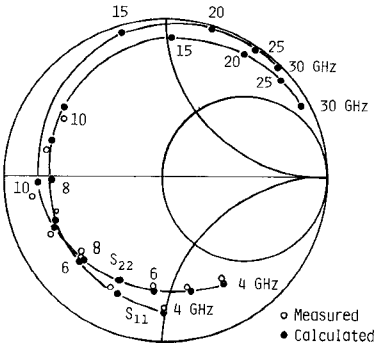


Fig. 5 S-parameters of the FET (S_{11} and S_{22}).

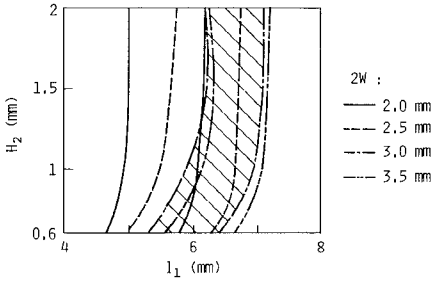


Fig. 6. Negative resistance region for the various mount dimensions at 28 GHz (Hatched region shows the negative resistance region in the case of $2W$: 3.0 mm.)

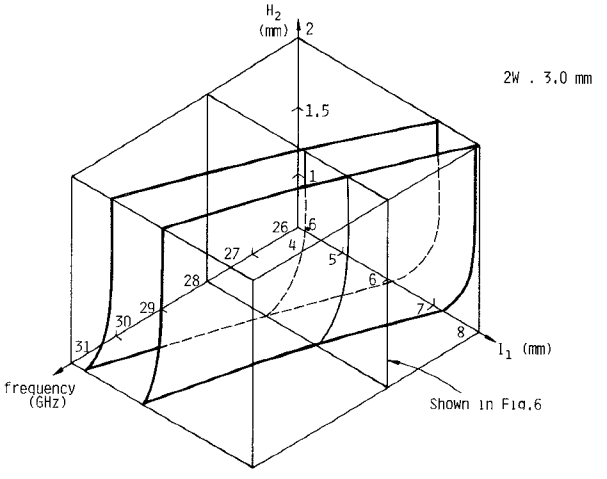


Fig. 7. Negative resistance characteristics frequency response with varying the mount dimensions (Calculation is carried out under the following conditions: 26 ≤ frequency (GHz) ≤ 31, 4 ≤ l_1 (mm) ≤ 8, 0.6 ≤ H_2 (mm) ≤ 2.)

dimensions. Fig. 7 shows one example of the negative resistance region when W is fixed.

Summarizing some calculations, the following results are obtained:

1) By shortening l_1, the negative resistance region is shifted into a higher frequency.

2) By widening W, the negative resistance region is shifted into a higher frequency. The variation by W is smaller than that by l_1 when $2 \leq 2W \leq 3.5$ mm, because Z_{gs} (shown in Fig. 3) depends more upon l_1 than Z_{lead} does, as discussed in Section III-A.

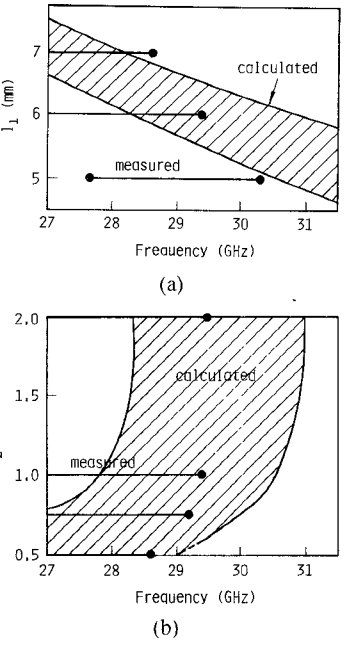


Fig 8. Negative resistance characteristics frequency response (measured). (a) Negative resistance region with varying l_1. (b) Negative resistance region with varying H_2.

3) By increasing H_2, the negative resistance region is shifted into a higher frequency. But the negative resistance region becomes constant when $H_2 \geq 1.0$ mm, because Z_{lead} becomes constant.

To confirm the above analysis, some experiments were carried out. Fig. 8 shows the experimental results. These experiments were in agreement with the above calculations.

C. Noise Performance

This section presents an experimental study on the relation between FET mount dimension and noise performance. The noise performance is evaluated by the noise measure (M).

The FET noise performance depends both on the dc bias conditions and the mount dimensions l_1, H_2, and W. The dc bias condition is set in accordance with the previously published results [7] and [8] which have shown that minimum noise performance is accomplished when $I_{ds} = 0.1 \sim 0.15 \cdot I_{dss}$; $V_{ds} = 3$ V; $I_{ds} = 5$ mA ($\approx 0.1 \cdot 55$ mA).

1) l_1 and W: Fig. 9 shows the noise measure with varying l_1 values. The minimum noise measure points shift with l_1. In this figure, the minimum point trace is drawn as a broken line. This line denotes the minimum noise measure, when the FET mount width $2W$ is 3.0 mm. In the frequency region from 27.5 GHz to 30 GHz, the noise measure is less than 6.5 ($M + 1 = 8.8$ dB). The FET mount width has little influence on the noise measure within $2 \leq 2W \leq 3$ mm.

2) H_2 Fig. 10 shows the noise measure with varying H_2. Here, FET mount width ($2W$) is 3.0 mm and H_1 is 4.0 mm. The bandwidth for low-noise measure is widened by increasing H_2. To obtain a wide-band and low-noise performance, it is sufficient to set $H_2 \geq 1$ mm.

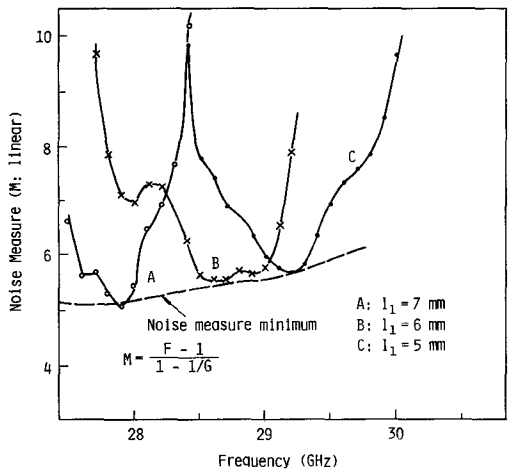


Fig. 9. Noise measure with varying l_1.

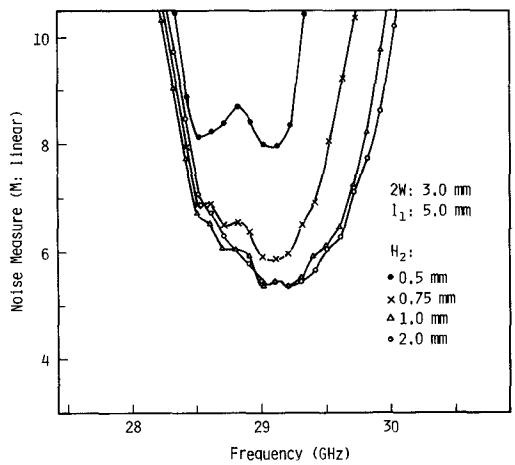


Fig. 10. Noise measure with varying H_2.

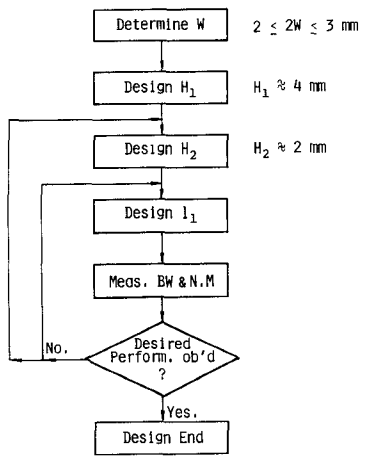


Fig. 11. FET mount design flow diagram.

D. Design Procedure

The effects of changing l_1, W, and H_2 on frequency and noise characteristics are clarified. The results are summarized in Table II. Fig. 11 shows a flow diagram for designing the FET mount.

TABLE II
MOUNT DIMENSION AND FREQUENCY RESPONSE, NOISE PERFORMANCE

Dimensions	Frequency response	Noise performance
l_1	By shortening l_1, the negative resistance region is shifted into a higher frequency.	By shortening l_1, Noise measure minimum point is shifted into a higher frequency.
W	By widening W, the negative resistance region is shifted into a higher frequency. Variation by W is smaller than that by l_1.	Noise measure minimum is almost unchanged, when 2W is 2 ~ 3 mm.
H_2	By increasing H_2, negative resistance region is shifted into a higher frequency. Variation by H_2 is smaller than that by l_1.	H_2 widens the low noise region.

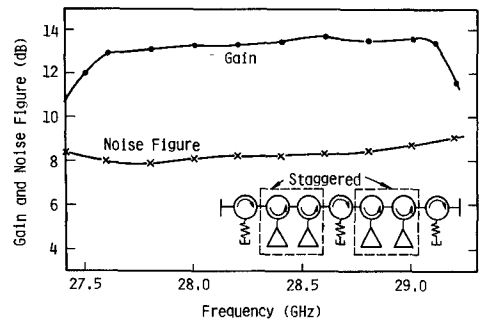


Fig. 12. 30-GHz band low-noise GaAsFET amplifier -1-.

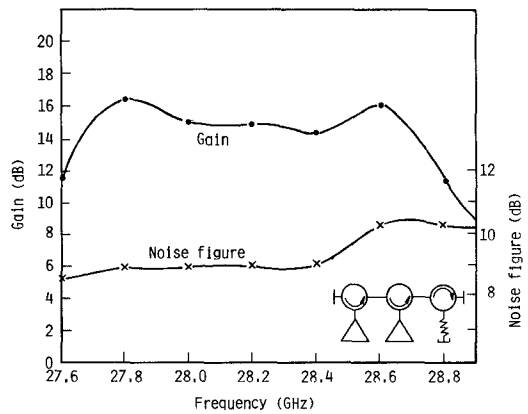


Fig. 13. 30-GHz band low-noise and high-gain GaAsFET amplifier -2-.

IV. Design Example of 30-GHz-Band Low-Noise Amplifiers

This section reports the design examples of two kinds of 30-GHz-band low-noise amplifiers. The first one is designed to achieve wide-band and low-noise performance. To obtain wide-band performance, four amplifiers are staggered. Electrical performance is shown in Fig. 12. In the frequency from 27.5 GHz to 29.1 GHz, 13 ± 1-dB gain is obtained. The noise figure for this amplifier is 8.5 ± 1 dB in the same frequency region.

The second one is designed to have high gain. To obtain high-gain performance, two amplifiers which have impedance transformers are cascaded. Fig. 13 shows the electrical

performance. The gain is 15 ± 1.5 dB in the frequency from 27.7 GHz to 28.7 GHz. The noise figure is 9 ± 1.5 dB.

V. Conclusion

A FET mount design method is established for 30-GHz-band low-noise amplifiers. Two design examples were shown using this method. One is 13-dB gain and 8.5-dB noise figure, the other is 15-dB gain and 9-dB noise figure.

Acknowledgment

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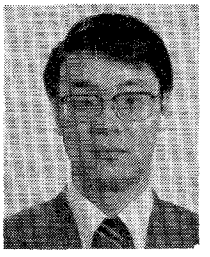

Hideki Mizuno was born in Niigata, Japan, on February 1, in 1952. He received the B.S. degree in electrical engineering from Tohoku University, Sendai, Japan, in 1975.

He joined the Yokosuka Electrical Communication Laboratory, Nippon Telegraph and Telephone Public Corporation, Yokosuka-shi, Kanagawa-ken, Japan, in 1975, and has since been engaged in research work on GaAsFET amplifiers for satellite communication systems. He is currently an Engineer of the Satellite Communication Equipment Section, Integrated Transmission System Development Division, Yokosuka Electrical Communication Laboratory.

Mr. Mizuno is a member of the Institute of Electronics and Communication Engineers of Japan.

Analysis of Image Recovery Down Converter Made by Planar Circuit Mounted in a Waveguide

YOZO UTSUMI, MEMBER, IEEE

Abstract—**This paper presents an analysis of a superhigh frequency (SHF) down converter using a Schottky-barrier mixer diode and a planar circuit mounted in a waveguide. The analysis assumes that the mixer diode consists of a nonlinear conductance g, a junction capacitance C_j, an ohmic spreading resistance R_s, and several parasitic susceptances. The frequency performance of the impedance of external circuits at the signal, image, and intermediate frequency bands is considered.**

This analysis also includes consideration of the mismatching effect between the converter and the IF amplifier, and the optimum design procedure for the down converter.

Using this theoretical method, a SHF down converter was designed and constructed. Its application is low-noise receivers for satellite broadcasting. The design used the optimum image condition (the image impedance takes a low value, i.e., nearly a short). The RF band is 11.7–12.2 GHz, the IF band is 0.96–1.46 GHz, and the total noise figure is 3.3–3.7 dB. The noise figure is in good agreement with the value (3.2–3.6 dB) obtained from this analysis.

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The author is with Technical Research Laboratories of Nippon Hoso Kyokai, 1-10-11, Kinuta, Setagaya-ku, Tokyo 157, Japan.

Nomenclature

g	Schottky junction nonlinear conductance of mixer diode.
C_j	Schottky junction capacitance of mixer diode.
$g_0 g_p g_{2p}$	Fourier expanded components of g.

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